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Efficient Gate Modulation in a Screening-Engineered MoS_2/Single-Walled Carbon Nanotube Network Heterojunction Vertical Field-Effect Transistor

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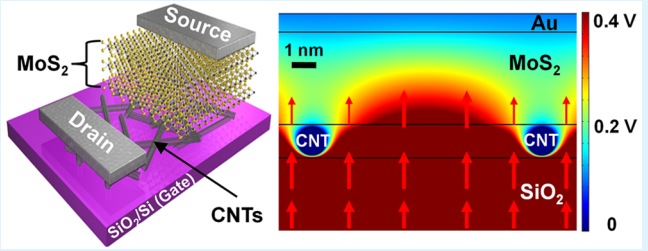
Supporting Information

ABSTRACT: In this report, a screening-engineered carbon nanotube (CNT) network/MoS_2/metal heterojunction vertical field effect transistor (CNT-VFET) is fabricated for an efficient gate modulation independent of the drain voltage. The gate field in the CNT-VFET transports through the empty space of the CNT network without any screening layer and directly modulates the MoS_2 semiconductor energy band, while the gate field from the Si back gate is mostly screened by the graphene layer. Consequently, the on/off ratio of CNT-VFET maintained 10^3 in overall drain voltages, which is 10 times and 1000 times higher than that of the graphene (Gr) VFET at V_{sd} = 0.1 (ratio = 81.9) and 1 V (ratio = 3), respectively. An energy band diagram simulation shows that the Schottky barrier modulation of CNT/MoS_2 contact along the sweeping gate bias is independent of the drain voltage. On the other hand, the gate modulation of Gr/MoS_2 is considerably reduced with increased drain voltage because more electrons are drawn into the graphene electrode and screens the gate field by applying a higher drain voltage to the graphene/MoS_2/metal capacitor.



KEYWORDS: *carbon nanotubes, graphene, molybdenum disulfide, vertical field-effect transistor, heterostructure*

INTRODUCTION

Graphene, a one-atomic-layer-thick carbon sheet, has attracted significant interest for application in electronic devices owing to its superior electrical conductivity,[1−4] high thermal conductivity,[5] and optical transparency.[6] However, the lack of band gap leads to low on/off current ratios of graphene-based devices in electronic applications. To address this challenge, a new class of atomically thin two-dimensional (2D) semiconducting materials, transition-metal dichalcogenides (TMDs), such as molybdenum disulfide (MoS_2),[7−11] molybdenum ditelluride ($MoTe_2$),[12] tungsten diselenide (WSe_2),[13] GaS, GaSe,[14] and black phosphorus (BP)[15] have been introduced. Owing to their sizable band gap characteristics,[7,16,17] the TMD materials can overcome the limitation of graphene and become most promising candidates to replace the conventional semiconducting materials such as silicon and germanium.

Owing to the weak van der Waals (vdW) interaction in the out-of-plane direction, the TMDs and graphene can be easily exfoliated and stacked into vdW heterostructures (vdWHs) regardless of the lattice mismatch, providing peculiar electronic and optoelectronic properties, verified in recent studies on vertical field-effect transistors (VFETs),[18−23] memory devices,[24−27] tunnel diodes,[28,29] photodetectors,[30−32] and solar cells.[33,34] Among them, graphene-based VFETs (Gr-VFETs) have attracted significant attention for next-generation electronic devices. The Gr-VFET was first introduced by us[19] and by the Manchester group,[35] while the barristor was introduced by Samsung group.[22] In VFETs, graphene electrodes, semiconductor channels, and metal electrodes are overlapped; therefore, electrons can largely flow through overall overlapping area.[19] Although, in barristor, on the other hand, graphene and semiconductor are overlapped but the metal electrode is not,[22] the electrons in the barristor have to flow through a very thin planar 2D TMD channel, inducing the limiting current flow. This is due to the weak electrostatic screening effect owing to the lack of density of states near the Dirac point of graphene enables gate modulation of the Schottky barrier at the vertical interface of the graphene and TMD heterojunction.[36] With a vertical current flow through the overlapping area of the vdWHs in the Gr-VFET, an ultrahigh current of 350 000 A cm^{-2} at a source−drain voltage

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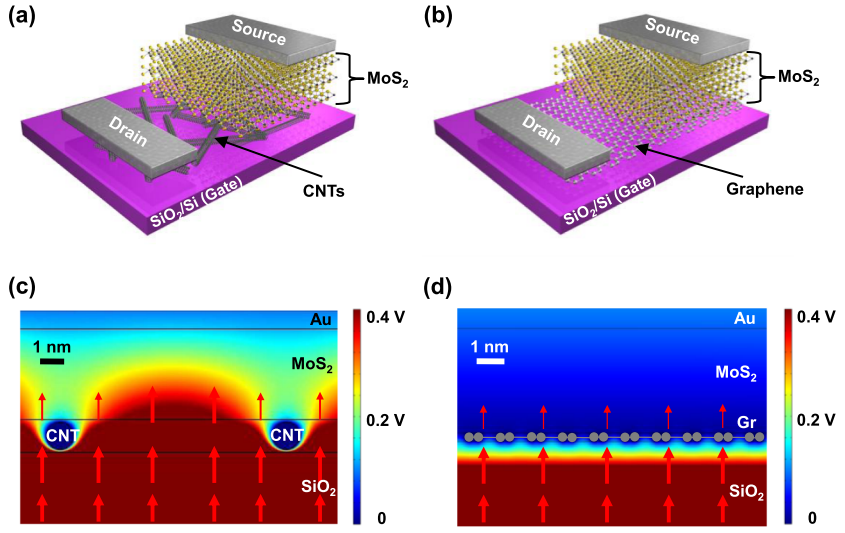

Figure 1. Three-dimensional schematics of the (a) CNT/MoS_2/metal (CNT-VFET) and (b) graphene/MoS_2/metal (Gr-FET) devices. (c,d) Corresponding electrostatic screening effect simulations of the gate electric field for the (a) m-SWCNT network and (b) graphene electrodes, respectively. The red arrows represent the electric field from the Si gate through the m-SWCNT (or graphene) electrode, MoS_2 channel, to the Au metal electrode.

(V_{sd}) of −4 V was achieved,[19,35] which is approximately 2 orders of magnitude larger than that of a planar TMD transistor with a limited thin planar TMD channel. However, the gate modulation in the Gr-VFET is significantly reduced with the increase in the drain voltage; the origin of this behavior has not been investigated. Furthermore, the gate coupling rate ($\beta = \Delta\Phi_{SB}/\Delta V_g$) between the Schottky barrier and gate voltage with a graphene screening layer was calculated to be 0.02, which is significantly smaller than that (0.2) of the structure without the graphene layer.[33]

Until now, most of the VFET studies reported on the level of qualitative analysis of device operation, consequently further optimization.[18,20,21] Here, we for the first time quantitatively explain the screening-engineered effect of VFET by using a single-walled carbon nanotube (SWCNT) as a bottom electrode instead of graphene. We identify the advantage of the SWCNT network, the empty space between the CNT−CNT junction, and attribute it to the gate transportation. In particular, the gate field in the CNT-VFET effectively transports through the empty space of the CNT network and then directly modulates the MoS_2 energy band at the CNT/MoS_2 contact.

In this paper, we report a screening-engineered SWCNT network/MoS_2/metal heterojunction VFET (CNT-VFET) for an efficient gate modulation in the whole drain bias range. Here, the on/off ratio in the gate modulation of the CNT-VFET exceeds 10^4 at a source−drain voltage (V_{sd}) of −0.5 V while that of the Gr-VFET with the graphene screening layer is 81.2 at the same V_{sd}. Furthermore, experimental and simulation results show that the Schottky barrier at the CNT/MoS_2 contact in the CNT-VFET can be independently modulated with the gate voltage in the whole drain bias range. On the other hand, the Schottky barrier at the graphene/MoS_2 contact (Gr-VFET) is hardly modulated at a high drain bias. This is because the drain voltage attracts the electrons in graphene and induced the Fermi level (E_F) of graphene shifts to the deep conduction band (CB) with a high density of state. Consequently, the on/off ratio of the CNT-VFET was maintained at 10^3 in the whole negative drain voltage range while that of the Gr-VFET was significantly reduced from 81.2 to 0.7 with the increase in V_{sd} from −0.5 to −2 V. Our approach could be employed for fabrication of one-dimensional (1D)−2D structures for future nanoelectronic and nanooptoelectronic devices.[37]

RESULTS AND DISCUSSION

Two different heterostructure configurations of VFETs are illustrated in Figure 1, consisting of a Au electrode on top, MoS_2 semiconducting channel in the middle part, and a metallic-SWCNT (m-SWCNT) network electrode (Figure 1a) or a graphene strip (Figure 1b) at the bottom part on a SiO_2/Si substrate. We estimate the electrostatic screening effects of the m-SWCNT network and graphene strip by a finite-element calculation using the COMSOL Multiphysics package (Figure 1c,d). The input parameters for the prototype materials, Si, SiO_2, air, CNT, graphene, and MoS_2 and gold (Au) electrode are presented in the Supporting Information Table S1.[31] In particular, graphene and CNT were treated as conductors for high carrier density material and the rest of the gap exist area was treated as dielectric.[38,39] In the simulation, the graphene and CNT were applied a bias of 0.1 V, while the top Au electrode was grounded and a Si back gate voltage of 3 V was applied. The color and red arrows shown in Figure 1c,d represent the fringing gate field potential and direction profiles, respectively. In the CNT-VFET (Figure 1c), the gate field efficiently transferred to the MoS_2 layer through the empty spaces between the m-SWCNTs. Furthermore, gate field fringing to MoS_2 on top of the m-SWCNTs is observed. In contrast, in the Gr-VFET (Figure 1d), the gate field from the Si back gate is mostly screened by the graphene layer. Only a small portion of the gate field is transferred to the MoS_2 layer (small red arrows) by penetration through the thin graphene layer. The simulation shows that the screening effect in the m-SWCNT network electrode is significantly lower than that in the graphene electrode, which implies a more efficient modulation of the gate field and high on/off current ratio of the CNT-VFET. However, this simulation is for brief estimation of the gate field penetration through graphene

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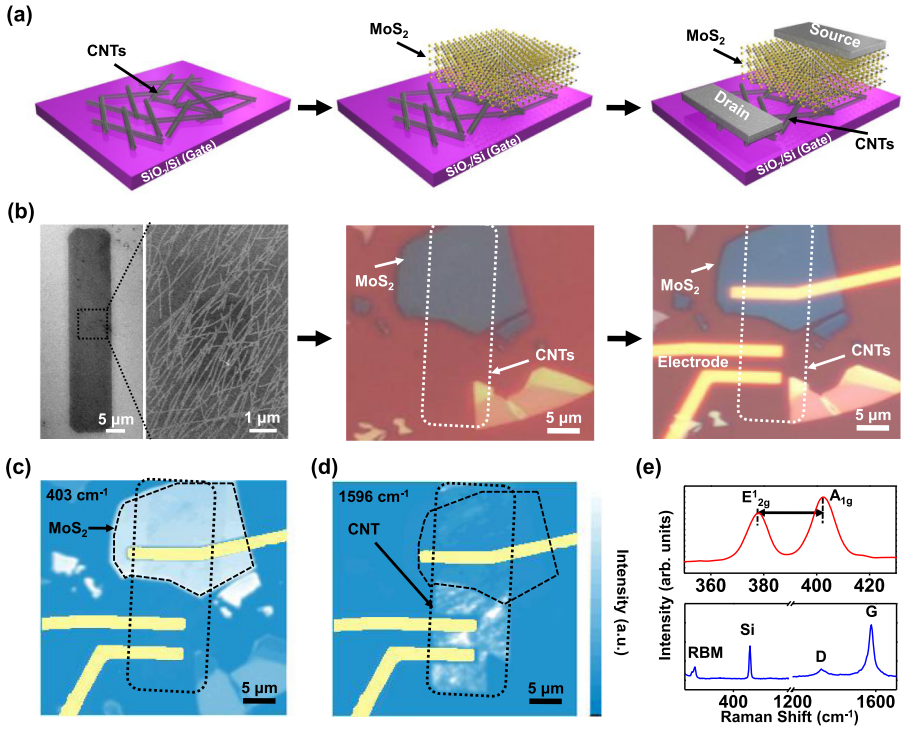

Figure 2. (a) Schematics of the fabrication steps for the CNT-VFET. (b) SEM and optical images corresponding to each step in (a). Raman maps of the peaks at (c) 403 cm^{-1} (MoS_2) and (d) 1596 cm^{-1} (CNT). (e) Raman spectra of MoS_2 (top panel) and CNT (bottom panel). The Raman mapping is carried out at a laser wavelength of 532 nm.

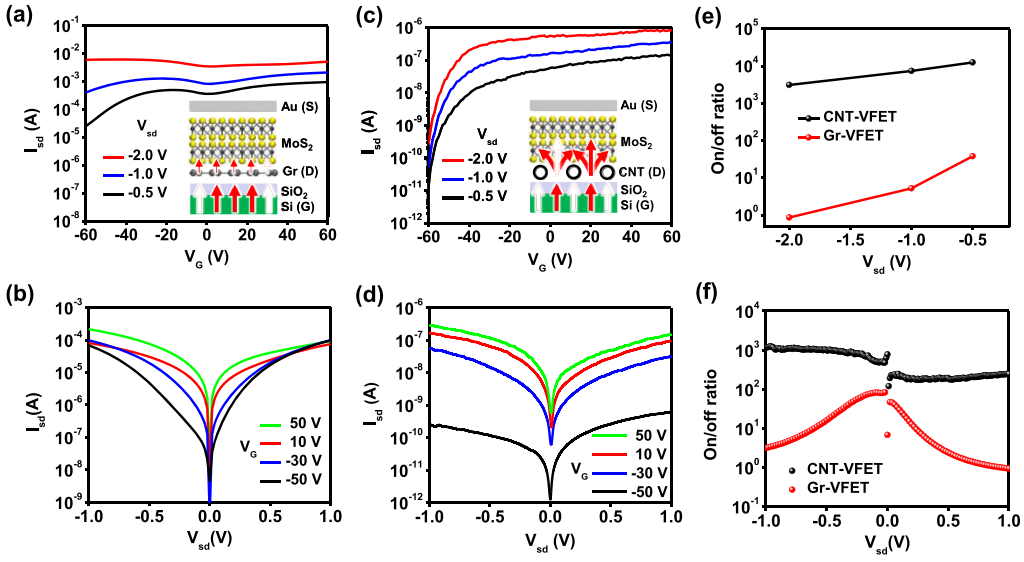

Figure 3. Transfer and output characteristics of the (a,b) Gr-VFET and (c,d) CNT-VFET at different source−drain biases in the range of −0.5 to −2 V and different gate biases in the range of −50 to 50 V, respectively. The insets in (a,c) show schematics of the Gr-VFET and CNT-VFET including the electric field directions, respectively. (e) On/off ratios of the CNT-VFET and Gr-VFET as a function of V_{sd} obtained using the curves in (a,c). (f) On/off ratios of the CNT-VFET and Gr-VFET as a function of V_{sd} obtained using the curves in (b,d).

and CNT film and the variable charge effect in graphene (or CNT film) is more deeply investigated in the energy band diagram simulation, which will be discuss later.

Figure 2a shows a schematic of the fabrication of the CNT-VFET. 99%-purified m-SWCNTs dispersed in a 1-methyl-2-pyrrolidinone (NMP) solution were spin-coated on a SiO_2 (300 nm)/Si wafer to form a CNT network and then patterned to CNT strips (10 × 50 μm^2) by the conventional photolithography method and O_2 plasma etching using a reactive-ion etching (RIE) machine. To fabricate the CNT/MoS_2 heterostructure, a MoS_2 flake was transferred onto the CNT network strips using a dry-transfer approach.[40] Finally, the metal electrodes were patterned on top of the MoS_2 and CNT network strip by e-beam lithography followed by e-beam/thermal deposition of Cr/Au (30/70 nm). Scanning electron microscopy (SEM) and optical images acquired at each fabrication step of the CNT-VFET are shown in Figure 2b. For the Gr-VFET, the same fabrication process was used,

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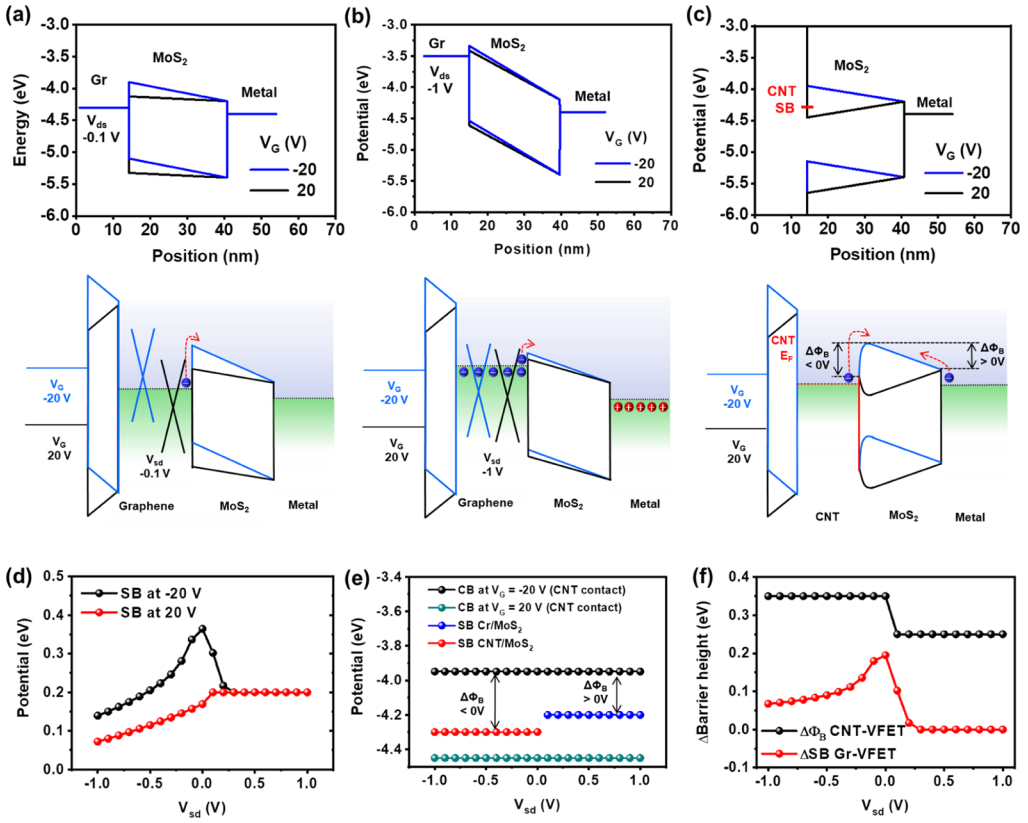

Figure 4. Simulated energy band diagrams of the Gr-VFET at V_{sd} of (a) −0.2 V and (b) −1 V at V_G = 20 and −20 V. (c) Simulated energy band diagrams of the CNT-VFET at V_G = 20 and −20 V. The bottom panel shows the corresponding schematic energy band diagrams. (d) Simulated Schottky barriers at the graphene/MoS_2 contact at V_G = 20 and −20 V. (e) Simulated CBs of MoS_2 at the CNT contact at V_G = 20 and −20 V, and Schottky barriers of CNT/MoS_2 and metal/MoS_2. (f) Schottky barrier variations of the CNT-VFET and Gr-VFET at various V_{sd} values.

except that a monolayer graphene grown by chemical vapor deposition was transferred onto a silicon (300 nm-thick SiO_2) substrate as the bottom electrode instead of the CNT network (Figure S1, Supporting Information). The device fabrication processes are presented in detail in Method section.

We characterized the MoS_2 and m-SWCNT heterostructure by Raman spectroscopy at an excitation laser wavelength of 532 nm, as shown in Figure 2c−e. The Raman mappings of the A_{1g} peak (403 cm^{-1}) for MoS_2 (black dashed line) and the G-peak (1593 cm^{-1}) for the CNT (black dotted line) are shown in Figure 2c,d, respectively. The overlapping area of MoS_2 and CNT is identified. The top panel of Figure 2e shows two peaks at ∼378 cm^{-1} (corresponding to the in-plane E^1_{2g} mode) and ∼403 cm^{-1} (corresponding to the out-of-plane A_{1g} mode), indicating the multilayer MoS_2.[41] The spectrum of the SWCNTs (bottom panel in Figure 2e) shows the radial breathing mode (RBM) peak at ∼123 cm^{-1}, indicating the m-SWCNTs according to the Kataura plot.[42] The metallic behavior of the prepared SWCNT network is confirmed by a gate-dependent electrical measurement (Figure S2, Supporting Information), where no considerable current change was observed upon a gate bias sweep.[43,44] The diameter of the m-SWCNT is calculated to be ∼2 nm using $\omega_{RBM} = 235.9/d_t + 5.5$,[45] where ω_{RBM} and d_t are the peak frequency and tube diameter, respectively. These results are consistent with the SEM, XRD, XPS, and UPS studies (Figures S3−S6, Supporting Information).

Figure 3 shows the electrical characteristics of the Gr-VFET and CNT-VFET. The supply voltage was applied to the bottom layer of the CNT (or graphene) electrode, while the top metal electrode was connected to the ground. The gate voltage was applied on the Si back gate (the insets in Figure 3a,c). Figure 3a,b shows the transfer and output characteristics of the Gr-VFET, respectively, with a MoS_2 channel thickness of 30 nm. The thickness of MoS_2 is similar to that in the CNT-VFET. The Fermi level of graphene in our device is slightly below the Dirac point (slightly *p*-doped) and effectively shifts by the gate bias in the transfer characteristics of the graphene electrode (Figure S7, Supporting Information). The conductivity of graphene, CNT, and MoS_2 is shown in Figure S8 and Table S2 (Supporting Information). The transfer characteristics of the Gr-VFET at various back gate voltages show that the current decreases with the increase in the negative gate voltage, demonstrating that the electrons are the majority charge carriers in this vertical transistor, which is consistent with the typical *n*-type semiconducting characteristics observed for MoS_2 materials.[7,19,46] The transfer characteristics of Gr-VFET shows the transition from *n*-type to *p*-type with an increase drain voltage at near V_G = 0 V because of the combined electrical characteristic of both MoS_2 and graphene (Figure S9, Supporting Information). It is worth noting that the on/off ratio of the Gr-VFET gradually decreases (81.2, 8.2, and 0.7) with the increase in V_{sd} (−0.5, −1, and −2 V, respectively) (Figure 3e). The reduction in the on/off ratio with the increase in V_{sd} is more obvious in the output characteristics of the Gr-VFET (Figure 3b) and extracted on/off ratio (the on-current at V_G = 50 V is divided by the off-current at V_G = −50 V in Figure 3b) at V_{sd} = −1 to 1 V (red dots in Figure 3f). The on/off ratio of the Gr-VFET significantly decreases from 83.3 to 1 with the increase in V_{sd}

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from 0.02 to 1 V. On the other hand, for the CNT-VFET, such an on/off ratio reduction with the increase in V_{sd} is not observed. Figure 3c shows the transfer characteristics of the CNT-VFET (I_{sd}–V_G) with a MoS_2 thickness of 29 nm [confirmed by an atomic force microscopy (AFM) measurement (Figure S10, Supporting Information]. V_{sd} biases of −0.5, −1, and −2 V were applied while the gate bias was swept from −60 to 60 V. Our CNT-VFET exhibited on/off ratios of 12 600, 7430, and 3110 at V_{sd} = −0.5, −1, and −2 V, respectively, approximately 1000 times higher than those of the Gr-VFET (Figure 3e). Furthermore, the on/off ratio of the CNT-VFET did not depend on the V_{sd} voltage. The output characteristics (I_{sd}–V_{sd}, Figure 3d) and extracted on/off ratio (black dots in Figure 3f) of the CNT-VFET more clearly show the independence between the on/off ratio and applied V_{sd} bias. The on/off ratios were 10^3 in the whole negative drain voltage range and 2×10^2 in the whole positive drain voltage range. It is noted that the diode rectifying behavior shown in Figure 3b,d is due to the asymmetric Schottky barrier heights between graphene (or CNT)–MoS_2 and metal/MoS_2.[47]

To investigate the difference in gate modulation between the CNT-VFET and Gr-VFET, we simulated the energy band diagrams at various gate voltages and corresponding Schottky barrier modulations using a model similar to previous reports[19,32] (Figure 4). It should be noted that the simulation results are purely indicative and only qualitatively valid. Figure 4a,b show the simulation results (top panel) and corresponding schematic energy band diagrams (bottom panel) of the Gr-VFET at V_{sd} of −0.2 and −1 V, respectively. At a low V_{sd} (−0.2 V in Figure 4a), the Fermi level in the graphene electrode is near the Dirac point. The gate field significantly changes the Schottky barrier of the graphene/MoS_2 contact owing to the lack of density of states near the Dirac point of graphene. At the high V_{sd} (−1 V in Figure 4b), the applied drain voltage attracts the electrons to the graphene electrode in the capacitor of graphene/MoS_2/metal, leading to the shift of E_F in the graphene to the deep CB. The Schottky barrier hardly changes in this state owing to the relatively high density of states. On the other hand, in the CNT-VFET (Figure 4c), the gate field effectively transports through the empty space of the CNT network and then directly modulates the MoS_2 energy band at the CNT/MoS_2 contact. In the simulation of CNT-VFET (S11, Supporting Information), therefore, the energy band modulation in MoS_2 in a given gate field is estimated in a gate/SiO_2/MoS_2/metal capacitor (top panel of Figure 4c). On the basis of simulation, we schematically draw the Schottky barrier at CNT/MoS_2 and band banding through MoS_2 (bottom panel of Figure 4c). The gate field causes an up- or down-bending of the MoS_2 bands, but the E_F of CNT and CNT/MoS_2 Schottky barrier remains unchanged.

Figure 4d shows the obtained Schottky barrier of the graphene/MoS_2 contact [work function (WF) of graphene (Φ_{Gr})–electron affinity of MoS_2 (X_{MoS_2})] at a V_G of −20 and 20 V in the V_{sd} range of −1 to 1 V, obtained by the simulation. The red dotted line in Figure 4f shows the Schottky barrier variation obtained by the difference in Schottky barrier between V_G = −20 and 20 V. At the negative V_{sd} in Figure 4f, the electrons flow from the graphene to the metal; therefore, the Schottky barrier at graphene/MoS_2 is dominant rather than MoS_2/Cr. Schottky barrier variation by the gate bias is observed at this state. According to Figure 3a,b, the Schottky barrier modulation is as low as 0.067 eV at V_{sd} = −1 V, which is gradually increased to 0.195 eV at $V_{sd} \approx 0$ V. However, at the positive V_{sd} in Figure 4f, the electrons flow from the metal to graphene. The Schottky barrier at MoS_2/metal is dominant rather than graphene/MoS_2 at this state. The fixed Fermi level of the metal induces the fixed Schottky barrier modulation at the MoS_2/metal contact. At very small positive V_{sd} values, Schottky barrier variation is observed as the gate-modulated built-in potential at the graphene/MoS_2 contact at a negative V_G is higher than the Schottky barrier of MoS_2/metal.

Figure 4e shows the key parameters of the CNT-VFET used to obtain the Schottky barrier. All parameters in our simulation are brought from references, see details in the Methods section. At a negative V_{sd}, the electrons flow from the CNT to the metal; therefore, the Schottky barrier at CNT/MoS_2 is dominant rather than metal/MoS_2 (see the schematics shown in Figure 4c). The CB of MoS_2 is increased to −3.95 eV (black dotted line shown in Figure 4e) at a positive V_G = −20 V by the direct application of the gate voltage through the empty area of the CNT network. The CB of MoS_2 at a positive V_G = +20 V (green dotted line shown in Figure 4e) is lower than the Schottky barrier of the CNT/MoS_2 (4.3 eV, red dotted line shown in Figure 4e). Therefore, the Schottky barrier modulation at a negative V_{sd} with the gate bias can be obtained to 350 meV from the difference between the CB of MoS_2 at V_G = −20 V and Schottky barrier of the CNT ($\Delta\Phi_B$ < 0 V shown in Figure 4e and black dotted line shown in Figure 4f). On the other hand, at the positive V_{sd}, the electrons flow from the metal to the CNT; therefore, the Schottky barrier at metal/MoS_2 is dominant (see the schematics shown in Figure 4c). The maximum CB of MoS_2 is still −3.95 eV at V_G = −20 V, while the minimum Schottky barrier of the metal/MoS_2 is 4.2 eV (blue dotted line shown in Figure 4e). Consequently, the Schottky barrier modulation by the gate bias can be obtained at 250 meV from the difference between the CB of MoS_2 at the CNT contact at V_G = −20 V and CB of MoS_2 at the metal contact ($\Delta\Phi_B$ < 0 V shown in Figure 4e and black dotted line shown in Figure 4f). It should be noted that the Schottky barrier modulations of the CNT-VFET and Gr-VFET shown in Figure 4f exhibit the same behavior as that of the on/off ratio variation shown in Figure 3e, which shows that our simulation is consistent with the current transports in the CNT-VFET and Gr-VFET. Furthermore, the calculated mobility was obtained as shown in Figure S12, (Supporting Information). By increasing the CNT density from 13 to 100 CNTs/μm^2, the mobility increased from 3.58 to 3.81 $cm^2\ V^{-1}\ s^{-1}$ (Figure S12a, Supporting Information).

Figure 5 shows the on/off ratios of the CNT-VFET and Gr-VFET at room temperature and V_{sd} = 0.5 V, under the gate bias sweep. The on/off ratios in both cases strongly depend on the thickness of the MoS_2 channel. In general, the on/off ratios of both CNT-VFET and Gr-VFET gradually decrease with the decrease in the MoS_2 thickness owing to the short-channel effect. With the decrease in the MoS_2 thickness, the electric field of the top metal electrode reduces the CB of MoS_2 and Schottky barrier height at graphene/MoS_2 or CNT/MoS_2 leading to a large off-current (the inset in Figure 5).[19] However, the CNT-VFET more effectively prevents the short-channel effect. Consequently, the on/off ratio of the CNT-VFET with a thick MoS_2 layer (~36 nm) exceeds 10^4, which is decreased to 6 for the very thin MoS_2 layer (4 nm) while that of the Gr-VFET is ~10^3 for a thick MoS_2 layer (~36 nm) and zero at a MoS_2 thickness of 10 nm. In all the cases, the on/off

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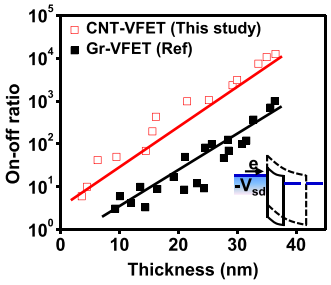

Figure 5. Comparison of the on/off current ratios of the CNT-VFET and Gr-VFET as a function of the MoS_2 thickness. The Gr-VFET data points are extracted from on/off ratio.[19] The solid lines are presented as visual guides.

ratios of the CNT-VFET are approximately 10 times higher than those of the Gr-VFET having the same MoS_2 thickness.

CONCLUSIONS

The m-SWCNT network enabled a new VFET design based on the vdWH with a high on/off ratio (>10^4) at room temperature compared to the Gr-VFET. Through systematic theoretical calculations and experiments, we showed that the independence between the gate modulation and drain voltage and the high gate modulation through the empty space of the CNT network were crucial to achieve the high-performance VFET. The dependence of the on/off ratio on the MoS_2 thickness was analyzed in detail. Compared to graphene-VFET, our CNT-VFET shows a smaller effective area that is critical for high current density and integration density. The current level of CNT-VFET can further increase by increasing the CNT density or doping density of CNT using a $AuCl_3$ dopant[48] (Figure S13, Supporting Information) or reducing the surface oxide in the contact area by annealing process (Figure S14, Supporting Information). Compared to conventional FETs, the actual current in our CNT-VFET shows 7.3 and 112.2 times higher current level than that of MoS_2 barristor and MoS_2 planar FET, respectively (Figure S15, Supporting Information). The achievement of a large current density is central to the performance of a VFET because the intrinsic delay of a transistor ($\tau = CV/I$) is inversely proportional to the deliverable current density.

We expect that our device is more useful for thin-film transistor (TFT) in active display, where the usual dimension of TFT is as large as 4 μm, which is easily achievable by using our CNT-VFET. The TFT in modern smart phone requires low off-current as well as high on/off ratio for low power consumption in a portable device. Our CNT-VFET can provide 10^5 times lower off-current and 10^3 times high on/off ratio than those of Gr-VFET. Other than that, the integration of logic circuit in vertical direction was demonstrated by stacking *n*-type and *p*-type VFETs,[19] providing the possibility of high integration to vertical way without small effective area. Our results demonstrated the potential of the m-SWCNT network as an exceptional electrode material for the fabrication of VFETs and further enhancement in the electronic device performance.

METHODS

Preparation of a CNT Solution. The m-SWCNTs containing 99% metallic CNTs were purchased from Nanointegris, USA (Iso-Nanotubes-M 99%). The CNT powder (2.4 mg) was dissolved and sonicated in 30 mL of NMP (99+%, spectrophotometric grade, Sigma-Aldrich) for 3 h in a bath-type sonicator (RK 106, BANDELIN Electronic, Germany) to obtain a CNT concentration of 80 μg/mL. The mixed solution was centrifuged to remove the remaining bundles in the solution at 13 000 rpm for 2 h (Supra 22K, Hanil Science Industrial Co., Ltd.). This solution was used to spin-coat the CNT channels.

Device Fabrication. Before the spin coating of the CNTs, a SiO_2 (300 nm)/Si wafer was immersed into a solution of 3-amino-propyltriethoxysilane (APTES, 99%, Sigma-Aldrich) and toluene for 30 min. The functionalized wafer was then used to spin-coat the CNTs (150 μL) at 4000 rpm. The devices were dried in a dry oven at 80 °C for 2 h. The conventional photolithography was used to fabricate CNT strips (10 × 50 μm^2). The unwanted CNT area was etched away by oxygen-plasma RIE (Miniplasma-Cube, PlaSmart) at 30 W for 30 s using a patterned photoresist by photolithography. MoS_2 flakes were then transferred onto the CNT strips using a dry-transfer approach. This method involved mechanical exfoliation of the MoS_2 flakes onto a dual-layer polymer stack of polyvinyl alcohol (PVA) and poly(methyl methacrylate). The bottom polymer (PVA) layer was dissolved in deionizer water. The resulting membrane was inverted and positioned above the target flake. The metal electrodes for the probe contact were patterned on MoS_2 and CNTs by e-beam lithography followed by e-beam deposition of Cr/Au (30/70 nm).

For the Gr-VFET, the same fabrication process was used, except that a monolayer graphene grown by chemical vapor deposition was transferred onto a silicon (300 nm-thick SiO_2) substrate as the bottom electrode instead of the CNT network.

Characterizations (AFM, Raman, SEM, and Electrical Measurements). AFM images were acquired using an E-sweep/Nano Navi Station scanning probe microscope (SII Nano Technology, Inc.). Raman spectroscopy was performed using a WITec system at an excitation wavelength of 532 nm. The field-emission SEM images were acquired using a JSM 7000F microscope (JEOL, Japan). Electronic transport measurements were carried out using a probe station and source/measure units (Keithley 4200) at room temperature under high-vacuum conditions (~1 × 10^{-6} Torr).

Energy Band Diagram Simulations. The charge distribution based on the Poisson's equation was solved in MATLAB, provided in S11, Supporting Information. The simulation was performed using the parameter from the references. In particular, the electron affinity of MoS_2 was 4.2 eV[49] and the work function of metallic CNT was 4.3 eV.[50]

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.9b05335.

Simulation of the electrostatic screening effects and energy band diagram of the CNT-VFET and Gr-VFET; characterization of the CNT (graphene) bottom electrode and MoS_2 film via electrical measurement, Raman spectroscopy, SEM cross-sectional view, XRD, XPS, and UPS; MoS_2 thickness measurement via AFM; electrical characterization of VFET due to the doping and annealing process; and calculations of the charge distribution and mobility of the VFET (PDF)

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The authors declare no competing financial interest.

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